EXHIBIT E

Paper No. __

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

GOOGLE LLC,
Petitioner,

v.

SINGULAR COMPUTING LLC,
Patent Owner.

Case No. IPR2021-00179
Patent No. 8,407,273

PETITION FOR INTER PARTES REVIEW
UNDER 35 U.S.C. §§ 311-319 AND 37 C.F.R. § 42.1 et seq.

In a typical binary (base-2) floating-point representation, one bit indicates the number's sign (positive or negative), some bits specify the "exponent" (the number's order of magnitude in base two), and other bits specify the mantissa. The number of exponent bits impacts dynamic range, the number of mantissa bits impacts precision, and there was a known tradeoff between the two. Ex. 1031, 191; Goodin, ¶¶ 29-30.

Benefits of LPHDR arithmetic were known in mathematics and computing. For example, Tong (Ex. 1008) recognized "wide dynamic range" as "a desirable feature," and explained "[i]t has long been known that many… applications can get by with less precision." Tong, 273; Goodin, ¶ 31. Tong demonstrated that certain applications could function properly with low-precision HDR arithmetic, and that lowering precision saved power by "reduc[ing] waste [from] unnecessary bits." Tong, 273, 277-279 ; Goodin, ¶¶ 32-34. Similarly, Dockser (Ex. 1007) disclosed a low-precision HDR execution unit that saved power by reducing precision in its floating-point operations to whatever precision was needed for a particular application. Dockser, [0003]-[0007]; Goodin, ¶ 35. The challenged claims encompass this prior-art concept and are unpatentable as demonstrated below.

II. SUMMARY OF GROUNDS

The challenged claims would have been obvious under § 103 as the following grounds demonstrate. Each reference below (none of which was before

the examiner) is prior art under pre-AIA § 102(b) even assuming the challenged claims were entitled to their earliest claimed priority date (they are not as Petitioner's concurrently filed petition demonstrates).

Ground Number and Reference(s)		Claims
1	Dockser (Ex. 1007)	1-2, 21-24, 26, 28
2	Dockser, Tong (Ex. 1008)	1-2, 21-24, 26, 28, 32-33
3	Dockser, MacMillan (Ex. 1009)	1-26, 28, 36-61, 63
4	Dockser, Tong, MacMillan	1-26, 28, 32-61, 63, 67-70

Ground 1: Dockser discloses a "floating-point processor" (FPP) that performs "multiplication" at a selectable "precision." Dockser, Abstract, [0012]. Dockser's FPP is an HDR execution unit whose standard floating-point inputs exceed the claimed minimum dynamic range, and which operates at a selectable reduced precision to conserve power in applications where greater precision is unnecessary. A selected "subprecision" is achieved by removing power to any desired number of least-significant mantissa bits, dropping those bits (resulting in less precision) and reducing power consumption. Dockser, [0014]; Goodin, ¶ 388-389. Dockser discloses an example that drops all but the 9 most-significant bits, resulting in imprecision meeting the claimed minimum error amounts. *Infra* § V.B.4.c. Dockser renders obvious claims 1-2, 21-24, 26, and 28.

Ground 2: Tong teaches reducing the number of mantissa bits to conserve power, and discloses experimental results demonstrating the optimum balance of precision and power consumption is achieved using just 5 mantissa bits for certain applications. *Infra* § VI.A. The Dockser/Tong combination, in which Tong's optimized precision levels are used in Dockser's LPHDR execution unit, renders obvious the same claims rendered obvious by Ground 1, and meets the claimed minimum error amounts by even greater margins. Tong teaches to emulate in software a device comprising an LPHDR execution unit; thus Dockser/Tong also meets independent claim 33.

Ground 3: MacMillan discloses a computer system with multiple floating-point execution units operating in parallel. *Infra* § VII.A. Based on MacMillan, a POSA would have been motivated to implement a device with multiple Dockser FPPs operating in parallel. The resulting device (Dockser/MacMillan) meets claims reciting multiple LPHDR execution units (including independent claim 36), and provides alternative bases for meeting the "device" in claim 1.

Ground 4: It would have been obvious to implement the Dockser/MacMillan device with the FPPs operating at Tong's precision levels. This Dockser/Tong/MacMillan combination meets the same claims met collectively by Grounds 1-3, and also claims 34-35 and 68-70, which recite a

parallel architecture (taught by MacMillan) and emulating the LPHDR execution units in software (taught by Tong).

III. STANDING

Petitioner certifies the '273 patent is available for IPR and Petitioner is not barred or estopped from requesting IPR of the challenged claims. 37 C.F.R. § 42.104(a).

IV. '273 PATENT

A. Independent Claims

The '273 patent includes independent claims 1, 33, 36, and 68. Claim 1 is reproduced below (annotated).

> [1A1] A device comprising: at least one first low precision high dynamic range (LPHDR) execution unit
>
> [1A2] adapted to execute a first operation on a first input signal representing a first numerical value to produce a first output signal representing a second numerical value,
>
> [1B1] wherein the dynamic range of the possible valid inputs to the first operation is at least as wide as from 1/65,000 through 65,000 and
>
> [1B2] for at least X=5% of the possible valid inputs to the first operation, the statistical mean, over repeated execution of the first operation on each specific input from the at least X % of the possible valid inputs to the first operation, of the numerical values represented by the first output signal of the LPHDR unit executing the first